WHAT IS CLAIMED IS:

1. A semiconductor device, comprising:

a substrate;

a first epitaxial layer formed on the substrate, the first layer having lattice mismatch relative to the substrate;

a second epitaxial layer formed on the first layer, the second layer having lattice mismatch relative to the first layer;

a third epitaxial layer formed on the second layer, the third layer having lattice mismatch relative to the second layer;

a first trench extending through the first layer;

a second trench extending through the third layer and at least partially through the second layer, at least part of the second trench being aligned with at least part of the first trench, and the second trench being at least partially filled with an insulating material.

2. The semiconductor device of claim 1, wherein part of the first trench extends through at least part of the second layer.

3. The semiconductor device of claim 1, wherein part of the first trench extends into the substrate.

4. The semiconductor device of claim 1, wherein the first trench is at least partially filled with the insulating material.

5. The semiconductor device of claim 1, wherein the first trench is at least partially filled with material of the second layer.

6. The semiconductor device of claim 1, wherein the first trench is at least partially filled with material of the third layer.

7. The semiconductor device of claim 1, wherein the second trench connects with the first trench.

8. The semiconductor device of claim 1, wherein the substrate is silicon.

9. The semiconductor device of claim 1, wherein the first layer comprises silicon germanium.

10. The semiconductor device of claim 1, wherein the second layer comprises relaxed silicon germanium.

11. The semiconductor device of claim 1, wherein the third layer is strained silicon.

12. The semiconductor device of claim 1, further comprising:

a transistor formed adjacent to the second trench and at least partially in the third layer.

13. A method of manufacturing a semiconductor device, comprising:

providing a substrate;

forming a first epitaxial layer on the substrate, wherein the first layer has lattice mismatch relative to the substrate;

forming a first trench in the first layer;

forming a second epitaxial layer on the first layer, wherein the second layer has lattice mismatch relative to the first layer;

forming a third epitaxial layer on the second layer, wherein the third layer has lattice mismatch relative to the second layer; and

forming a second trench in the third and second layers, wherein at least part of the second trench is in alignment with at least part of the first trench.

14. The method of claim 13, wherein the substrate is silicon.

15. The method of claim 13, wherein the first layer comprises silicon germanium.

16. The method of claim 13, wherein the second layer comprises relaxed silicon germanium.

17. The method of claim 13, wherein the third layer is strained silicon.

18. The method of claim 13, wherein the first trench extends at least partially through the first layer.

19. The method of claim 18, wherein the first trench extends through the first layer and into the substrate.

20. The method of claim 13, wherein material of the second layer at least partially fills the first trench.

21. The method of claim 13, wherein the second trench connects with and opens to the first trench.

22. The method of claim 13, further comprising:

at least partially filling the second trench with an insulating material; and

if the second trench opens to the first trench and the first trench is not completely filled, filling an open remainder of the first trench with the insulating material.

23. The method of claim 13, further comprising:

forming a transistor adjacent to the second trench, wherein at least part of the transistor is formed in the third layer.

24. The method of claim 13, wherein the first layer is deposited at a deposition temperature, and further comprising:

after forming the first trench, annealing the first layer at about 100° C higher than the deposition temperature.

25. The method of claim 13, further comprising:

planarizing the first layer prior to forming the second layer.

26. The method of claim 13, further comprising:

planarizing the second layer prior to forming the third layer.

27. A semiconductor device produced using the method of claim 13.

28. A method of manufacturing a semiconductor device, comprising:

providing a substrate;

forming a first epitaxial layer on the substrate, wherein the first layer has lattice mismatch relative to the substrate;

forming a second epitaxial layer on the first layer, wherein the second layer has lattice mismatch relative to the first layer;

forming a first trench in the second and first layers;

forming a third epitaxial layer on the second layer, wherein the third layer has lattice mismatch relative to the second layer; and

forming a second trench in the third and second layers, wherein at least part of the second trench is in alignment with at least part of the first trench.

29. The method of claim 28, wherein the third layer is strained silicon.

30. The method of claim 28, wherein the first trench extends through the second layer and into the first layer.

31. The method of claim 30, wherein the first trench extends through the second layer, through the first layer, and into the substrate.

32. The method of claim 28, wherein the second trench connects with and opens to the first trench.

33. The method of claim 28, further comprising:

at least partially filling the second trench with an insulating material; and

if the second trench opens to the first trench and the first trench is not completely filled, filling an open remainder of the first trench with the insulating material.

34. The method of claim 28, further comprising:

forming a transistor adjacent to the second trench, wherein at least part of the transistor is formed in the third layer.

35. A semiconductor device produced using the method of claim 28.